

LPDT μ L 9040, 9041 AND 9042

LOW POWER DIODE TRANSISTOR MICROLOGIC[®]

INTEGRATED CIRCUITS

GENERAL DESCRIPTION

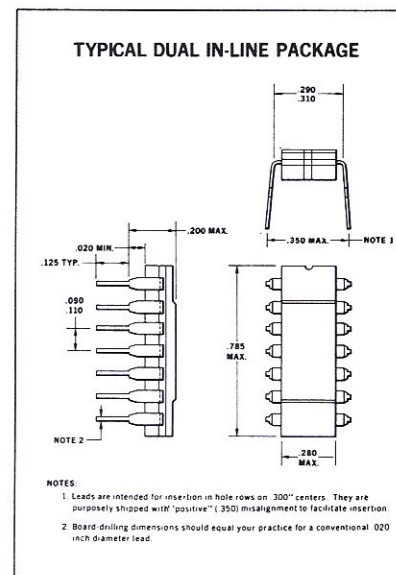
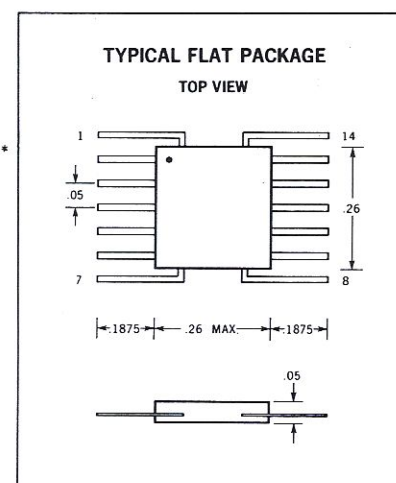
The Fairchild LPDT μ L Micrologic[®] Integrated Circuit Family consists of a set of compatible, integrated logic circuits specifically designed for low power, medium speed applications.

The circuits are fabricated with a silicon monolithic substrate using standard Fairchild Planar* epitaxial processes.

Packaging options include the Flat package and the Dual In-Line package.

Important features of the LPDT μ L Micrologic[®] integrated circuits include the following:

- Reliable operation over the full military temperature range of -55°C to +125°C
- Typical power drains of less than 1 mW per gate (50% duty cycle) for the logic gate elements and less than 4 mW for the clocked flip-flop.
- Single power supply requirement—5 volts optimum, 4.5 to 5.5 volts range.
- Guaranteed fan-out of 10 LPDT μ L unit loads or 1 standard Fairchild DT μ L unit load, over the full temperature and supply voltage range.
- Guaranteed minimum of 450 mV noise immunity at the temperature extremes.
- Typical logic gate propagation delays of 60 ns and binary clock rate of 2.5 MHz.
- Emitter follower outputs providing good capacitive drive capability.



*Planar is a patented Fairchild process.

ORDER INFORMATION

To order Low Power Diode Transistor Micrologic[®] integrated circuit elements specify U31XXXX51X for flat package and U6AXXX51X for Dual In-Line package where XXXX is 9040, 9041 or 9042.

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD
SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

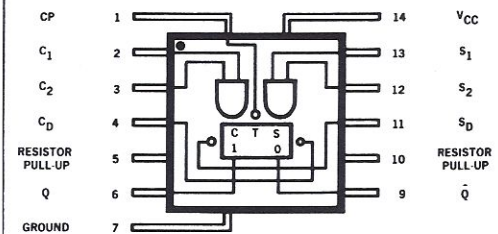
FAIRCHILD MICROLOGIC® LOW POWER DIODE TRANSISTOR INTEGRATED CIRCUITS

LPDT μ L 9040 CLOCKED FLIP-FLOP

DESCRIPTION

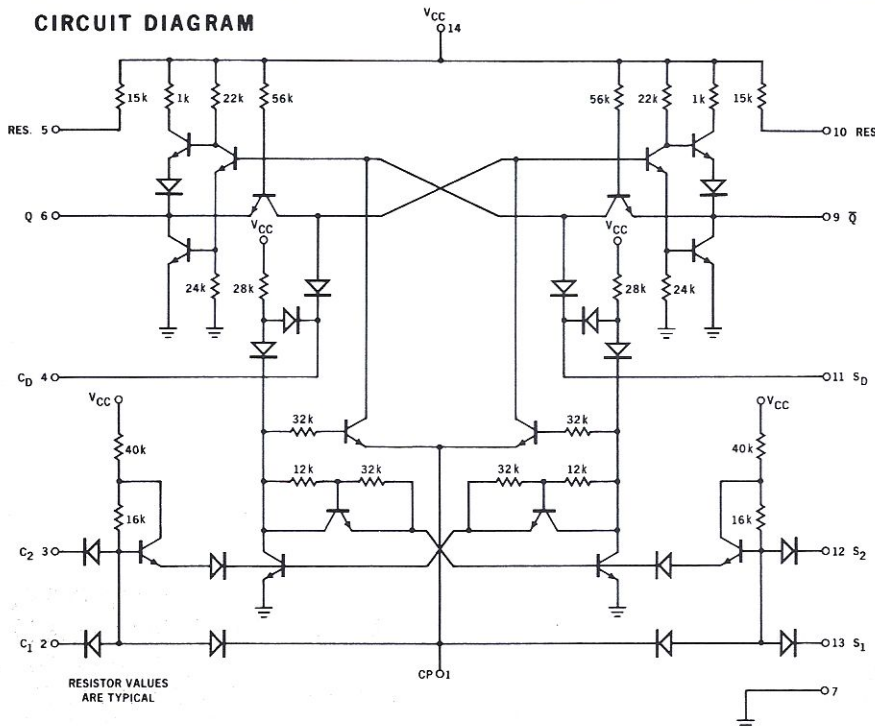
The LPDT μ L 9040 element is a directly coupled, dual-rank flip-flop suitable for use in counters, shift registers and other storage applications. Either R-S or J-K mode operation is possible. Direct set and clear inputs are provided which override all other data inputs.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN LINE PACKAGE PIN ASSIGNMENT



SYNCHRONOUS ENTRY TRUTH TABLES										ASYNCHRONOUS ENTRY TRUTH TABLE			
R-S MODE OPERATION						J-K MODE OPERATION				TRUTH TABLE			
INPUTS @ t_n				OUTPUTS @ t_{n+1}		INPUTS @ t_n		OUTPUTS @ t_{n+1}		INPUTS		OUTPUTS	
S_1	S_2	C_1	C_2	Q	$\bar{Q}$	S_1	C_1	Q	$\bar{Q}$	S_D	C_D	Q	$\bar{Q}$
13	12	2	3	6	9	13	2	6	9	11	4	6	9
L	X	L	X	NC	NC	L	L	NC	NC	H	H	NC	NC
L	X	X	L	NC	NC	L	H	L	H	H	L	L	H
X	L	L	X	NC	NC	H	L	H	L	L	H	H	L
X	L	X	L	NC	NC	H	H	TOGGLES		L	L	H	H
L	X	H	H	L	H	Symbols H - Most positive logic level L - Most negative logic level X - Either H or L can be present NC - No change in state							
X	L	H	H	L	H								
H	H	L	X	H	L								
H	H	X	L	H	L								
H	H	H	H	AMBIGUOUS									
						NOTES: 1. For J-K mode operation connect Pin 6 to Pin 3 and Pin 9 to Pin 12. 2. Asynchronous entries override all synchronous entries.							

CIRCUIT DIAGRAM



LOADING RULES

INPUT	*NORMALIZED UNIT LOADS (U.L.)
S_1 S_2 C_1 C_2	0.75 U.L.
S_D C_D	2.5 U.L.
CP	2.5 U.L.
OUTPUT	FAN-OUT
$Q, \bar{Q}$	10 U.L. 7 U.L. WITH RESISTOR PULL-UP CONNECTED

*1 UNIT LOAD EQUALS 1-LPDT μ L 9041 OR 9042 INPUT LOAD

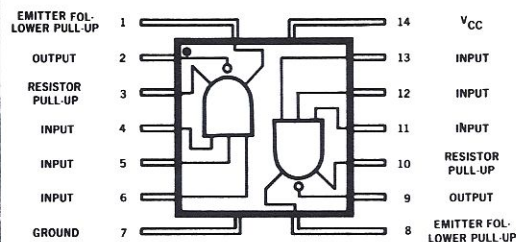
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LPDT μ L 9041 – DUAL 3 INPUT NAND GATE

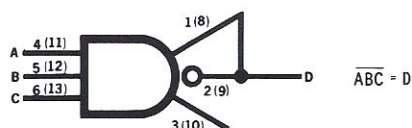
DESCRIPTION

The LPDT μ L 9041 element consists of two, 3-input positive logic NAND gates suitable for general logic gate and inverter applications. The unique feature of this gate is that the output transistor collector and the emitter follower pull-up are not internally connected. This allows the user to tie collectors to a common node for the wired "OR" logic function.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT



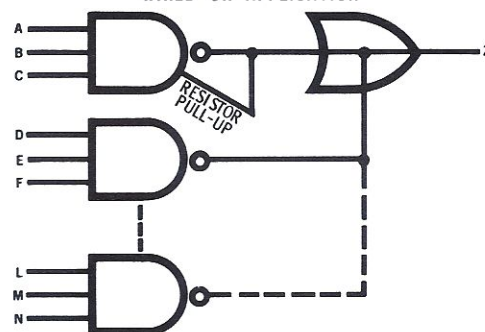
POSITIVE LOGIC NAND GATE



EACH INPUT = 1 UNIT LOAD
OUTPUT FAN-OUT = 10 UNIT LOADS
= 7 U.L. WITH RESISTOR
PULL-UP CONNECTED

EITHER THE EMITTER FOLLOWER OR RESISTOR PULL-UP
MUST BE CONNECTED TO THE OUTPUT TO ESTABLISH
THE HIGH LEVEL.

WIRED 'OR' APPLICATION

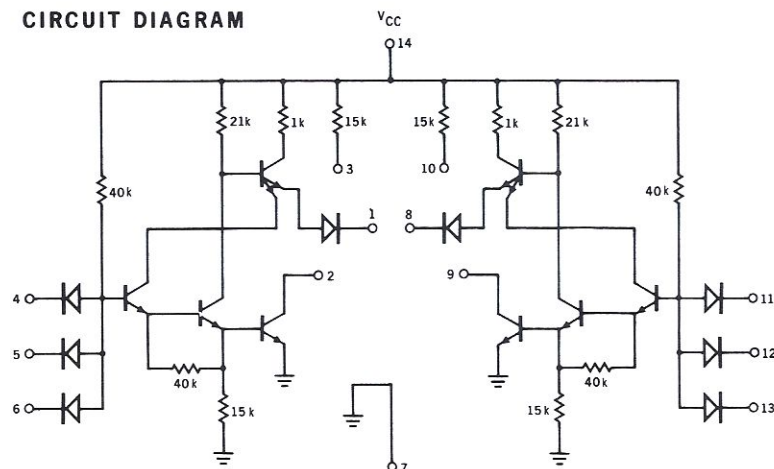


$$ABC + DEF + \dots + LMN = Z$$

OUTPUT FAN-OUT = 10 - 3 (NO. OF RESISTOR
PULL-UPS)

ONE PULL-UP RESISTOR IS REQUIRED FOR EVERY 8
GATES CONNECTED TO THE COMMON "OR" NODE.

CIRCUIT DIAGRAM



RESISTOR VALUES
ARE TYPICAL

FAIRCHILD MICROLOGIC® LOW POWER DIODE TRANSISTOR INTEGRATED CIRCUITS

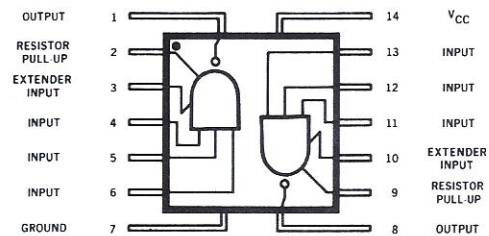
LPDT μ L 9042 — DUAL 3 INPUT NAND GATE WITH EXTENDER INPUTS

DESCRIPTION

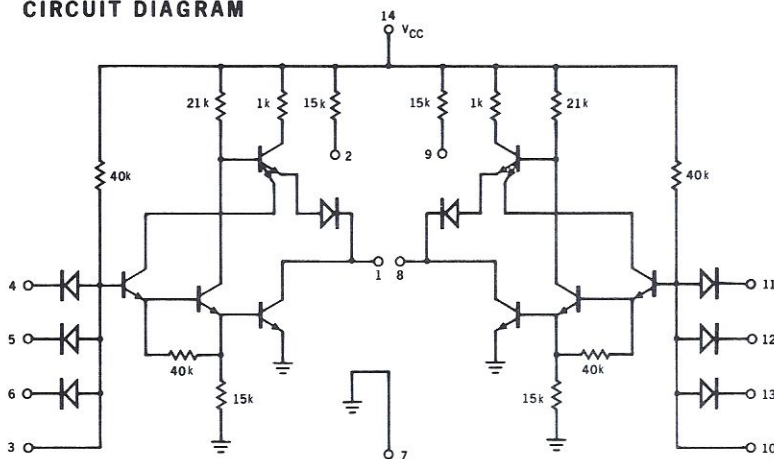
The LPDT μ L 9042 element consists of two 3-input positive logic NAND gates with extender inputs. This element in the family allows the user to implement logic applications requiring a gate fan-in exceeding three.

The DT μ L 9933 4-input extender element or equivalent—may be used to provide additional diode inputs. Any capacitance added to the extender input will increase the turn-on delay of the LPDT μ L 9042 gate. Typically, the increase is 10 ns/pico-farad. Turn-off delay is not affected.

LOGIC DIAGRAM SHOWING FLAT OR DUAL-IN-LINE PACKAGE PIN ASSIGNMENT

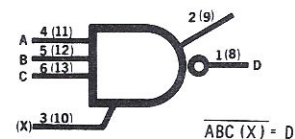


CIRCUIT DIAGRAM



RESISTOR VALUES
ARE TYPICAL

POSITIVE LOGIC NAND GATE



EACH INPUT = 1 UNIT LOAD
OUTPUT FAN-OUT = 10 UNIT LOADS
= 7 UNIT LOADS WITH
RESISTOR PULL-UP
CONNECTED

BUFFER ELEMENT

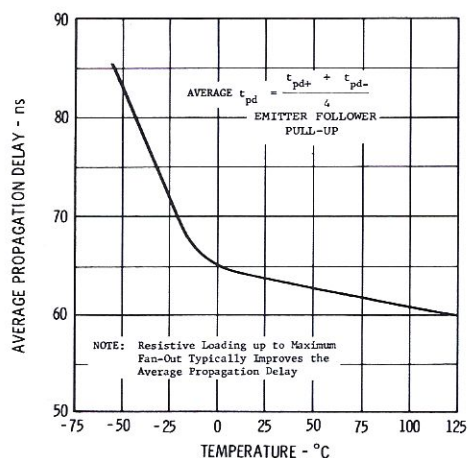
For applications requiring a fan-out exceeding ten, the Fairchild DT μ L 9930 Dual 4-Input Gate may be used. The DT μ L 9930 will drive 44 LPDT μ L unit loads, while maintaining the same output logic levels as the low power circuits.

The input of a DT μ L 9930 requires the equivalent of 10 LPDT μ L unit loads. Therefore, a low power circuit can drive only one DT μ L 9930 input.

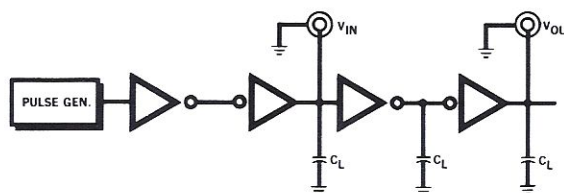


FAIRCHILD MICROLOGIC® LOW POWER DIODE TRANSISTOR INTEGRATED CIRCUITS

**TYPICAL
AVERAGE PROPAGATION DELAY
LPDTμL 9041•9042**



TEST CIRCUIT



CONDITIONS

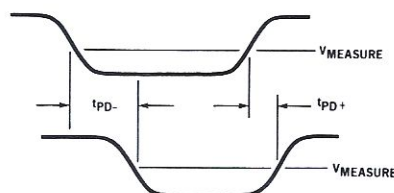
$V_{CC} = 5.0V$, $C_L = 50pF$ (INCLUDING PROBE AND JIG CAPACITANCE)

$V_{MEASURE} = 1.6V @ -55^{\circ}C$

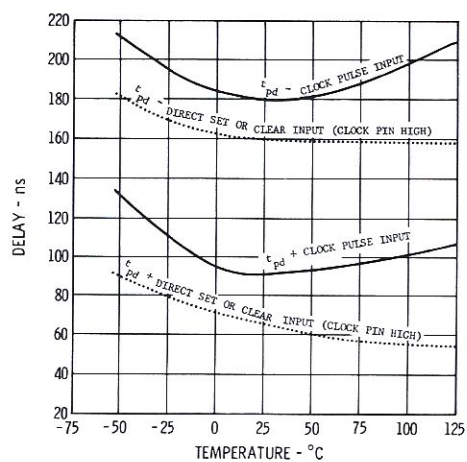
(GND. REF.) $1.3V @ 25^{\circ}C$

$0.9V @ 125^{\circ}C$

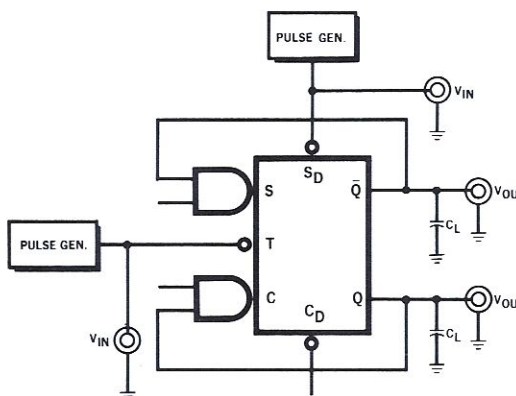
WAVE FORMS



**TYPICAL DELAY CHARACTERISTICS
LPDTμL 9040**



TEST CIRCUIT



CONDITIONS

$V_{CC} = 5.0V$, $C_L = 50pF$ (INCLUDING PROBE AND JIG CAPACITY)

$V_{MEASURE} = 1.6V @ -55^{\circ}C$

(GND. REF.) $1.3V @ 25^{\circ}C$

$0.9V @ 125^{\circ}C$

WAVE FORMS

